SCiCoreDrive22

2 channel IGBT driver

ADVANCE INFORMATION

HIGHLIGHTS

- 2 channel IGBT driver.
- Suitable for 1200 V IGBT (900 V max on DC-Link).
- 2 modes of operation: direct mode or half bridge mode.
- 0-5 V or 0-15 V input level signaling.
- Configurable dead time generation.
- Short pulse suppression.
- Collector sensing & fault protection.
- Electrical isolation of 3000 $V_{AC.}$
- Built-in DC-DC converter.

non-contractual picture

APPLICATIONS

- Inverters.
- Converters.
- Renewable energies.
- Traction.
- Welding.
- UPS.

ABSTRACT

SCiCoreDrive22 is a general purpose 2-channel driver designed to control IGBTs up to 1200 V. Incorporates a built-in flyback converter capable of supply an output power of 5 W (2.5 W per channel). Includes an V_{CE} monitoring of IGBT, it lets the protection of this one in case of failure by soft turning off the IGBT, and sending an optically isolated feedback fault signal. **SCiCoreDrive22** can work in two different modes: direct mode, is the same as having two independent drivers, or the half-bridge mode, specially designed to drive the 2 IGBT of the same half-bridge (top and bottom) generating the required dead times (configurable by the user).The **SCiCoreDrive22** signal inputs are Schmidt–trigger, and admit logic levels of 0-5 V or 0-15 V (selectable by the user). The signal inputs also includes a short pulse suppressor to avoid undesired glitches and parasites.

The built-in flyback converter is primary regulated, so any little variations in its supply voltage does not means variations of turn-on and turn-off voltage levels at the outputs, only implies variations in the current consumption.

The driver output stage is designed with 2 bipolar transistors in totem pole configuration. It has 2 outputs (RON and ROFF) instead the usual GATE output. It provides better performance in the case of using different resistors (asymmetrical gate control) for turn-on and turn-off without the need of output diodes.

This driver is suitable for most common topologies including half-bridges, full-bridges or three phase bridges of IGBTs with a DC-Link up to 900 V covering a wide range of applications: inverters, converters, renewable energies, traction, welding, UPS.

101019 Rev:6

POWER SUPPLY

Symbol	Description	Conditions & notes	min.	typ.	max.	units
V_{CC}	Supply voltage		13	15	17	V
I_{CC}	Current consumption (full load)	Q_G=0.80 µC, f_{sw}=100 kHz (2 chan.)			480	mA
I_{STBY}	Stand by consumption (no load)			140		mA

LOGIC INPUTS/OUTPUTS

Symbol	Description	Conditions & notes	min.	typ.	max.	units
V_{IN_H}	IN signal high level	See LOGIC LEVELS			15	V
V_{IN_L}	IN signal low level	See LOGIC LEVELS	0			V
I_{FAULT_L}	FAULT current				8	mA

TIMING CHARACTERISTICS

Symbol	Description	Conditions & notes	min.	typ.	max.	units
$t_{d\ ON}$	High output propagation time	***figure 1***			2.4	µs
$t_{d\ OFF}$	Low output propagation time	***figure 1***			2.6	µs
$t_{d\ FAULT}$	Desat. detection to FAULT output delay	***figure 2***		1.8	5	µs
t_{blank}	Blanking time	***figure 2***			2.8	µs
$t_{d\ DES(10)}$	Desat. detection to 10% turn off	***figure 2***		0.3	0.5	µs
$t_{d\ DES(90)}$	Desat. detection to 90% turn off 90%	***figure 2***		2	3	µs
$t_{d\ RES\_FAULT}$	Reset to fault	***figure 2***	3	7	20	µs
PW_{RES_min}	Minimum pulse width for RESET		0.1			µs
f_{sw_max}	Max. Switching frequency	***note 1***			100	kHz
DC	Duty cycle for IN_x signals	***note 2***	0		100%	

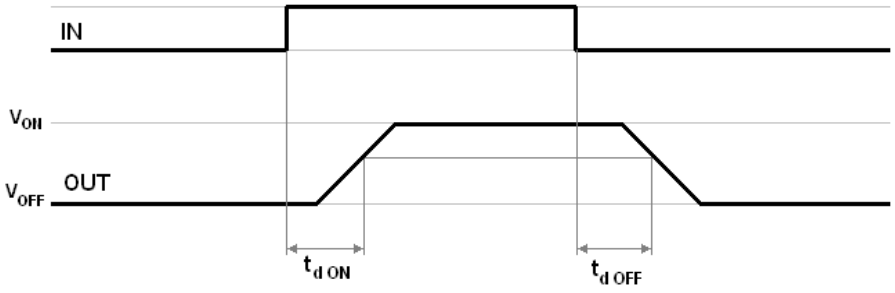


figure 1: *input-output chronogram*

note 1: Maximum switching frequency is limited by the formula:

$$f_{sw} \le \frac{I_{OUT\_AV\max}}{Q_G}$$

note 2: Minimum pulse to the IN_x inputs is 1.8 µs (see SHORT PULSE SUPRESSION).

POWER OUTPUTS

Symbol	Description	Conditions & notes	min.	typ.	max.	units
f_{DC-DC}	Built-in converter switching frequency			285		kHz
P_{TOT}	Output power (total)			5		W
P_{CHAN}	Output power per channel			2.5		W
V_{ON}	Turn ON gate voltage output	R_G=22 R, Q_G=0.80 µC, f_{sw}=10 kHz	13.5	15		V
V_{OFF}	Turn OFF gate voltage output			-15	-13.5	V
$I_{out\ peak(+)}$	Output peak positive current				16	A
$I_{out\ peak(-)}$	Output peak negative current				-16	A
$I_{out\ Avmax}$	Output average current	each channel			83	mA
R_{GON_min}	Minimum resistance value to R_{ON} output	**note 3**			2	Ω
R_{GOFF_min}	Minimum resistance value to R_{OFF} output	**note 3**			2	Ω
$Q_{Gmax/PLS}$	Maximum charge at IGBT gate per pulse				6	µC
T_{p_min}	Minimal pulse suppression	see SHORT PULSE SUPRESSION			1.4	ms

ELECTRICAL ISOLATION

Symbol	Description	Conditions & notes	min.	typ.	max.	units
$V_{ISO\ P-S}$	Isolation voltage between primary to secondary	50 Hz (1 min)	3000			V_{AC}
$V_{ISO\ S-S}$	Isolation voltage between channels	50 Hz (1 min)	1000			V_{AC}
V_W	Safety IGBT working voltage				900	V

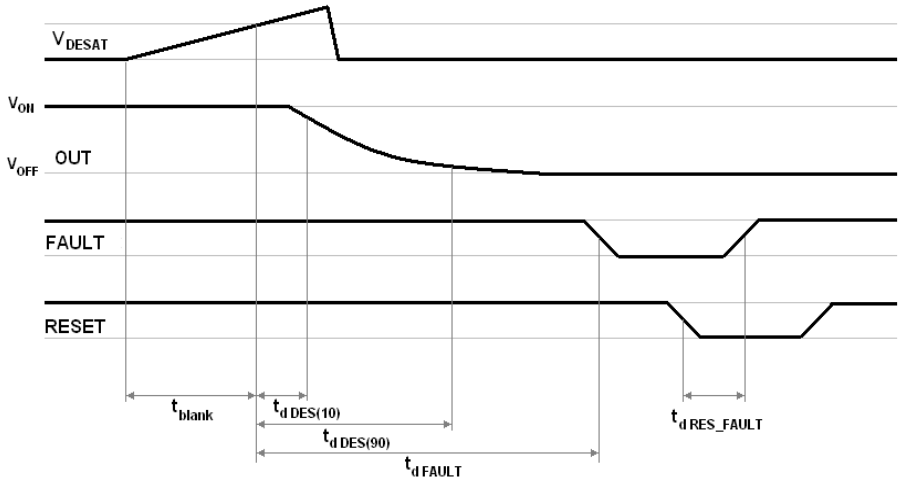
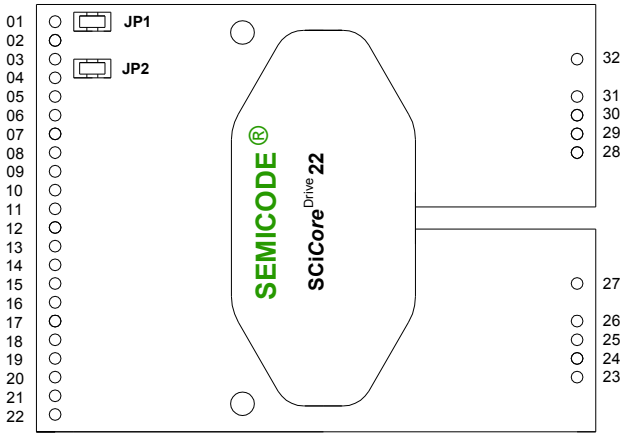


figure 2: *desaturation and failure detect chronogram.*

note 3: R_G includes internal gate resistance of the IGBT module.

$$I_{outpeak} = \frac{V_{GON} - V_{GOFF}}{R_G + R_{G\,\mathrm{int}(MODULE)}}$$

PINOUT



Primary side

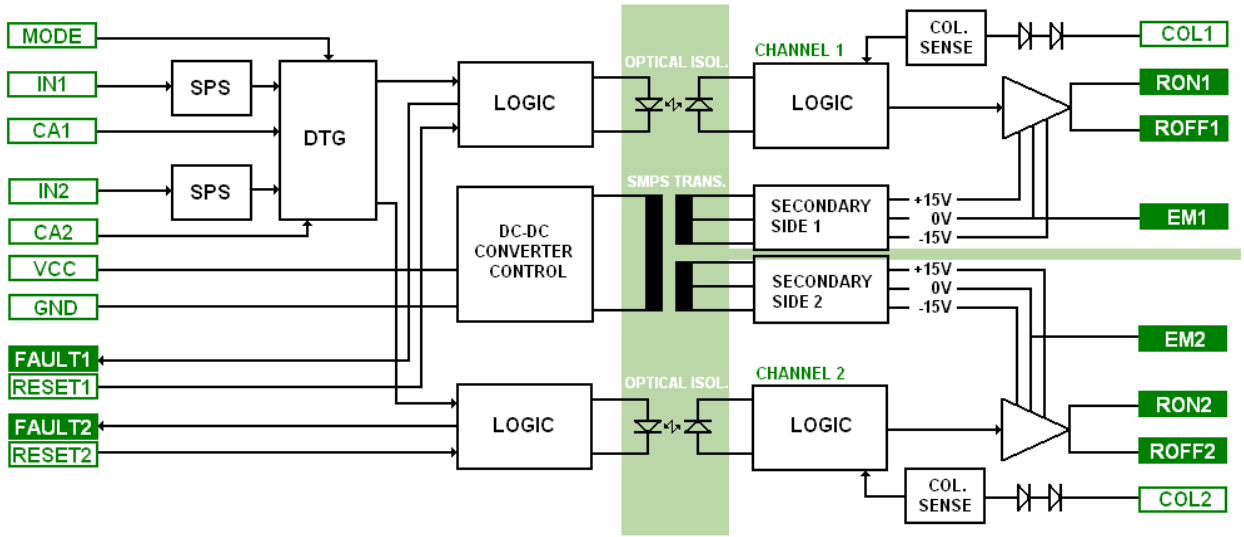
#pin	Name	Description
1	VCC	15 V for general supply voltage
2	VCC	15 V for general supply voltage
3	VCC	15 V for general supply voltage
4	VCC	15 V for general supply voltage
5	VCC	15 V for general supply voltage
6	VCC	15 V for general supply voltage
7	IN1	Signal input channel 1
8	CA1	Capacitor for DTG
9	FAULT1	Fault output channel 1
10	RESET1	Reset input channel 1
11	MODE	Input mode
12	NC	Not connected
13	IN2	Signal input channel 2
14	CA2	Capacitor for DTG
15	FAULT2	Fault output channel 2
16	RESET2	Reset input channel 2
17	GND	Ground for supply & input signals
18	GND	Ground for supply & input signals
19	GND	Ground for supply & input signals
20	GND	Ground for supply & input signals
21	GND	Ground for supply & input signals
22	GND	Ground for supply & input signals

Secondary side

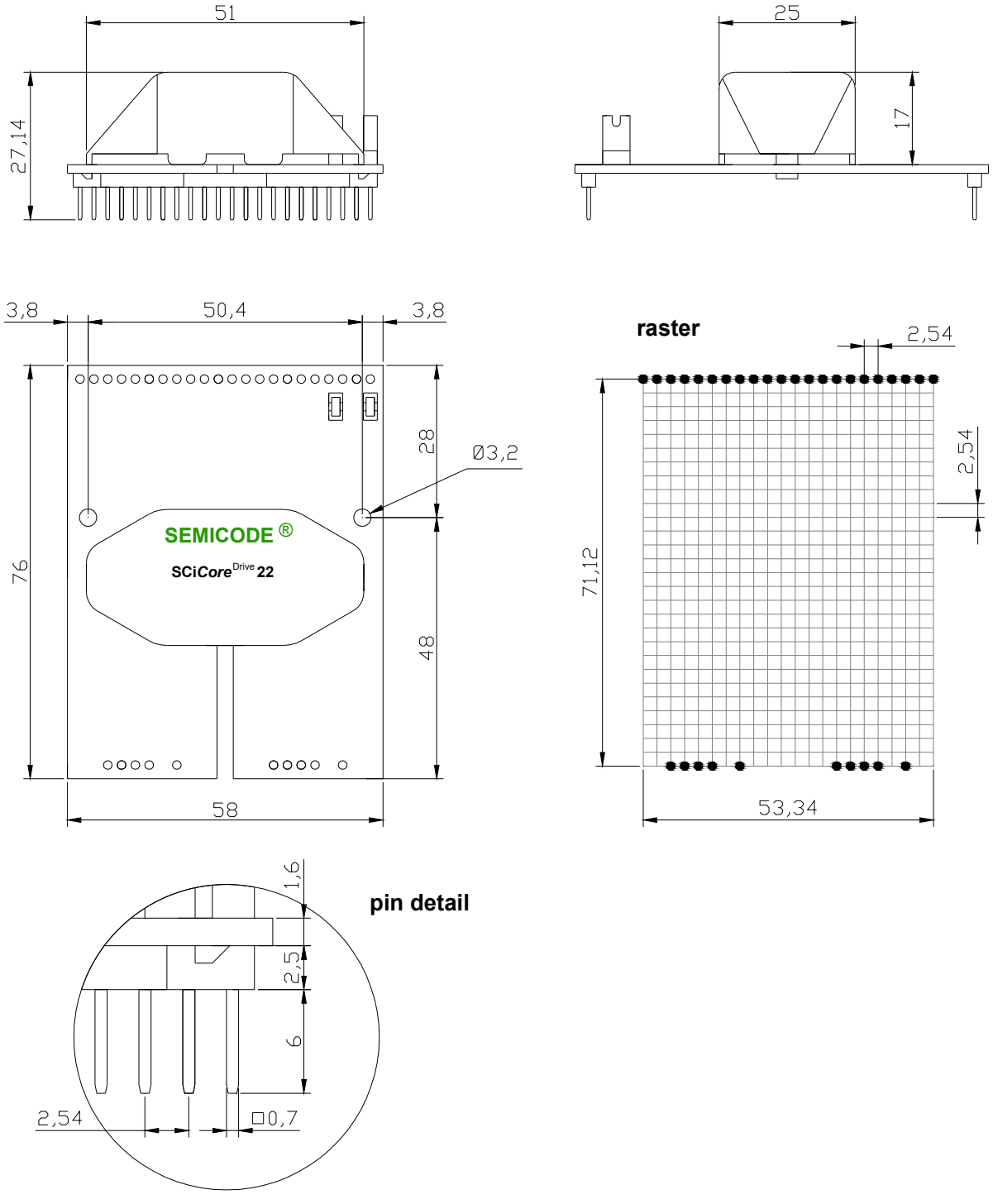
#pin	Name	Description
23	EM2	Emitter 2
24	EM2	Emitter 2
25	ROFF2	Gate 2 resistor for OFF pulse
26	RON2	Gate 2 resistor for ON pulse
27	COL2	Collector sense channel 2
28	EM1	Emitter 1
29	EM1	Emitter 1
30	ROFF1	Gate 1 resistor for OFF pulse
31	RON1	Gate 1 resistor for ON pulse
32	COL1	Collector sense channel 1

#jumper	Description
JP1	Jumper for logic level IN1 selection
JP2	Jumper for logic level IN2 selection

BLOCK DIAGRAM



MECHANICAL DIMENSIONS



All dimensions in millimeters

APPLICATION: DRIVING SINGLE IGBT

SCiCoreDrive22 is an easy-to-use driver, that require only a few quantity of additional components to drive correctly the IGBT with ±15 V at the gate. We must apply to IN_x the signal that would be transferred to the output_x of the driver for turn-on and turn-off the power IGBT_x. FAULT_x is an open-collector output that indicates with low level if a failure occurs in the system driver+IGBT. RESET_x is the input for rebooting the channel_x and FAULT_x signal (see FAILURE MANAGEMENT).

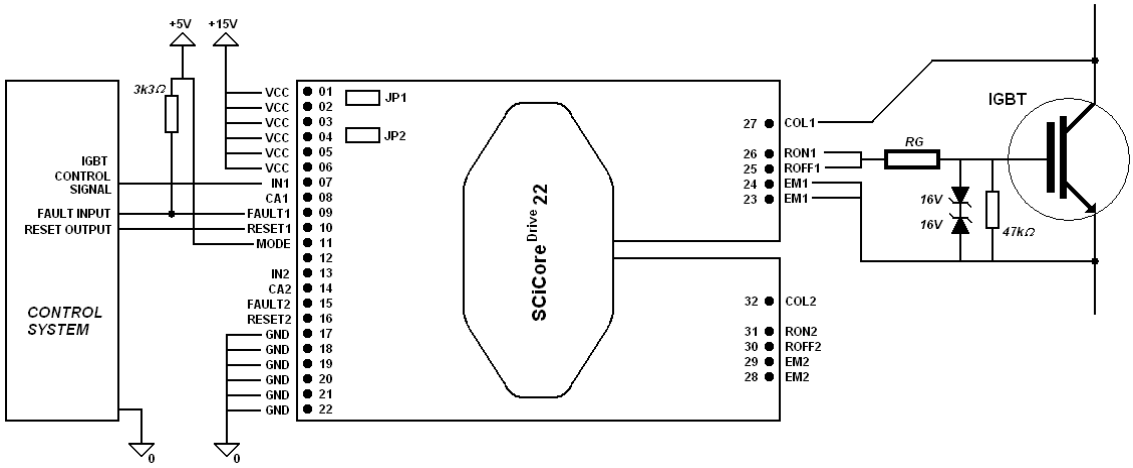


figure 3

TRUTH TABLE

IN_x	*RESET_x*	*Failure detected*	*FAULT_x*	*VOUT_x (*)*
HIGH	HIGH	NO	HIGH	V_{ON}
LOW	HIGH	NO	HIGH	V_{OFF}
x	HIGH	YES	LOW	V_{OFF}
x	LOW	NO	HIGH	V_{OFF}

* VOUT_x refers the voltage between RON/ROFF_x and EM_x

LOGIC LEVELS

The inputs of **SCiCoreDrive22** (IN_x, RESET_x and MODE) are TTL compatible. The FAULT_x outputs are open collector outputs, and require an external pull-up resistor (see figure 3).

Symbol	*Description*	*Signal & conditions*	*min.*	*max.*	*units*
$V_{i\_HIGH\_R\_M}$	Input signal voltage for high level	RESET, MODE	2	5	V
$V_{i\_LOW\_R\_M}$	Input signal voltage for low level	RESET, MODE	0	0.8	V
$V_{i\_HIGH\_IN}$	Input signal voltage for high level	IN_x (JP1&JP2 plugged)	3.7	5	V
$V_{i\_LOW\_IN}$	Input signal voltage for low level	IN_x (JP1&JP2 plugged)	0	1.3	V
$V_{i\_HIGH\_IN}$	Input signal voltage for high level	IN_x (JP1&JP2 Unplugged)	11	15	V
$V_{i\_LOW\_IN}$	Input signal voltage for low level	IN_x (JP1&JP2 Unplugged)	0	3.9	V

In addition, the inputs IN_x are schmitt-trigger and admits 2 different levels depending on whether the JP1 & JP2 are plugged or not. We recommend to use the 0-15V levels for a better noise immunity. Is not permitted to use different level configuration on each channel. Both channels must work as 0-15 V or 0-5 V. Using 0-15 V input signal when jumpers JP1 & JP2 are plugged can damage the driver.

SHORT PULSE SUPRESSOR (SPS)

Each Input signal (IN_x) of **SCiCoreDrive22** includes a SPS to protect the driver and the IGBT from undesired short duration glitches. A pulse shorter than 1.4 µs will be eliminated with 100% probability. A pulse longer than 1.8 µs will pass the SPS without suffer any change. A pulse with a duration between 1.4 µs and 1.8 µs may pass or not.

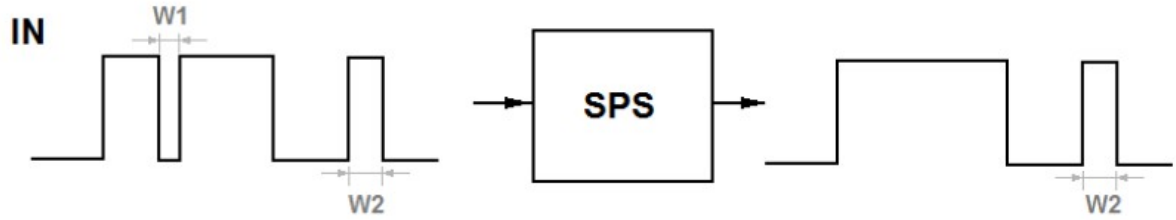


figure 4

FAILURE MANAGEMENT

The power stage of a typical three phase inverter or full bridge is susceptible to several types of failures, most of which are potentially destructive to the power IGBT. Under any of these fault conditions, the current through the IGBT can increase rapidly, causing excessive power dissipation and heating. The IGBT become damaged when the current load approaches the saturation current of the device, and the collector to emitter voltage rises above the saturation voltage level. The drastically increased power dissipation overheats very quickly the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn-off the over-currents during a fault condition. **SCiCoreDrive22** provides fast local fault detection and shutdown.

The fault detection method is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false 'fault' signals.

During normal operation, voltage at RON_x and ROFF_x is controlled by the signal IN_x, with the IGBT collector to emitter voltage being monitored through V_{DESAT}. The FAULT output is high and the RESET input must be held high.

Warning Note:
By default SCiCoreDrive22 is supplied set as 0-5 V TTL inputs level configuration mode (Jumpers J1 and J2 connected). Please check your application needs; **driving 0-15 V level to the inputs when the board is configured at 0-5 V can damage the driver**.

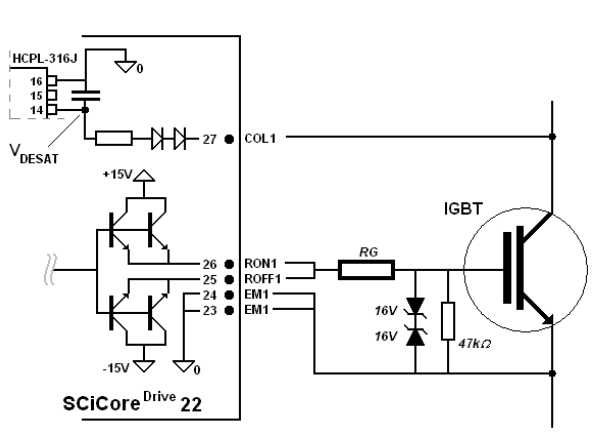


figure 5: Internal circuitry of SCiCoreDrive22

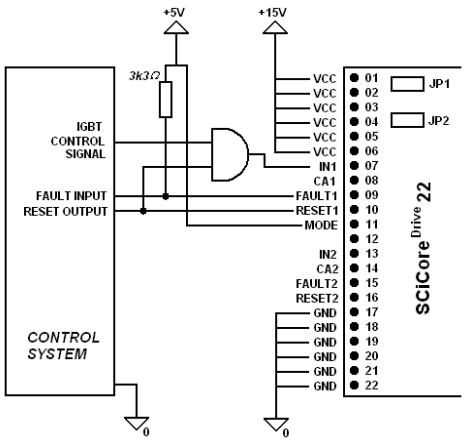


figure 6: Possible implementation of «safe hardware RESET»

When the voltage on V_{DESAT} exceeds 7 V while the IGBT is ON, V_{OUT} (refers to V_{RON}/V_{ROFF} to V_{EM} voltage) is slowly brought low in order to «softly» turn-off the IGBT and prevent large di/dt induced voltages. Also activated is an internal feedback channel which brings the FAULT output low for the purpose of notifying the control system (see figure 5). The FAULT outputs remains low until RESET is brought low. While asserting the RESET_x to low, the input signals (IN_x) must be asserted for an output low state (0 V). This may be accomplished either by software control or hardware control (see figure 6).

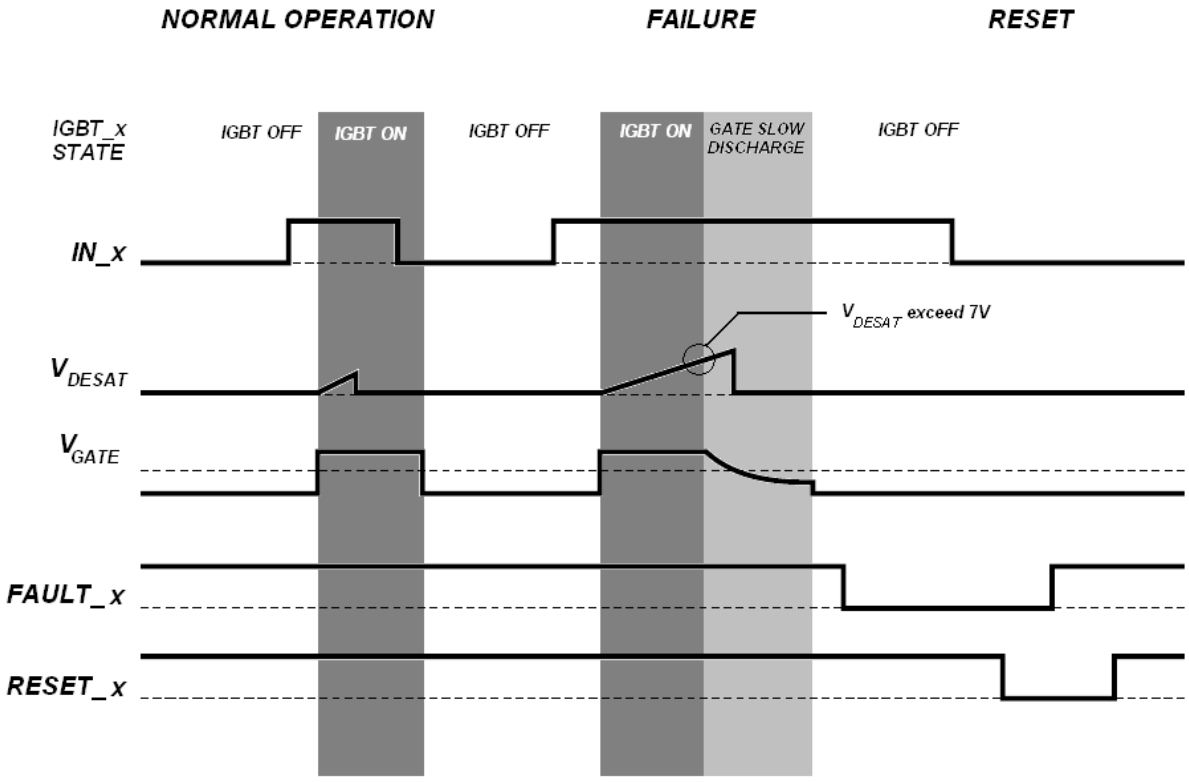
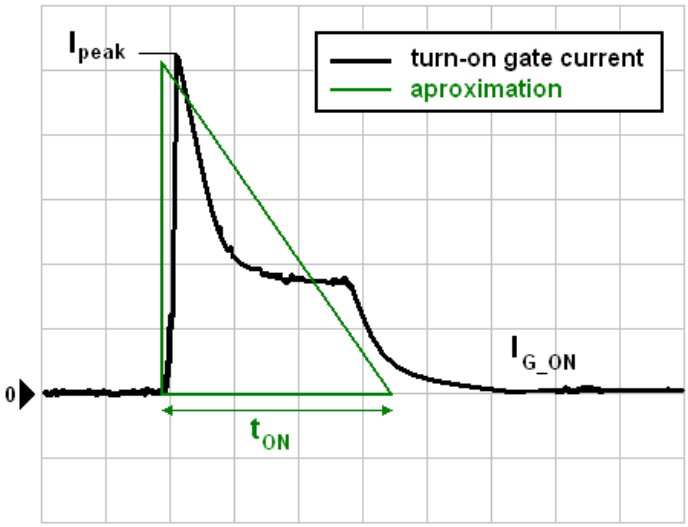


figure 7

DETERMINING GATE CAPACITANCE OF THE IGBT

The most important parameter to determine the switching times of the power IGBT is the gate capacitance. The value printed in the IGBT datasheet as «C_{iss}» cannot be used for all applications, and do not corresponds to the effective input gate capacitance. For our particular application, the best way to calculate the gate capacitance is obtaining the gate charge. Gate charge may be obtained by measuring the gate current, for this purpose, the IGBT must be driven by driver.



The waveforms obtained should be as this ones:

$$Q_G = \int I_G dt$$

Gate charge can be calculated as:

$$Q_G = \frac{I_{peak} \cdot t_{ON}}{2}$$

if the approximation is used:

$$C_G = \frac{Q_G}{V_{GON} - V_{GOFF}}$$

then the gate capacitance is:

figure 8: *gate current waveform, and lineal approximation.*

SCiCoreDrive22 drives the IGBT with ±15 V so V_{GON}-V_{GOFF} = 30 V.

RESISTOR GATE DIMENSIONING

The switching behavior of power semiconductors is controlled by the gate capacitance recharge. This gate capacitance recharge may be controlled via a gate resistor. The dynamic IGBT performance can be adjusted by the value of the gate resistor. The gate resistor influences the IGBT switching time, switching losses, reverse bias safe operating area (RBSOA), short-circuit safe operating area (SCSOA), EMI, dv/dt, di/dt and reverse recovery current of the freewheeling diode. It has to be selected very carefully.

Increasing the resistor value involves to increase the turn-on and turn-off time, and the switching losses of the IGBT, but reduces the turn-on/turn-off peak current, the di/dt, voltage spikes and EMI noise. Final application will decide the most important parameters to increment or reduce RG, the only limitation imposed from driver is the maximum gate peak current permitted

Minimum gate resistor is given by the formula:

$$R_{G\min} = R_G + R_{G\text{int}(MODULE)} \frac{V_{GON} - V_{GOFF}}{I_{\max\_peak}} = \frac{30V}{16A} = 1{,}87\Omega$$

SYMMETRICAL OR ASYMMETRICAL GATE CONTROL

What needs to be considered when reducing the value of the gate resistor is the di/dt generated when high currents are switched too fast. This is due to stray inductance present in the circuit, which produces a high voltage spike on the IGBT. This effect can be observed during IGBT turn-off.

The transient voltage spike on top of the collector-emitter voltage may destroy the IGBT, especially in short-circuit turn-off operation with a high di/dt., V_{stray} can be reduced by increasing the value of the gate resistor. Thus, the risk of IGBT destruction due to overvoltage can be eliminated.

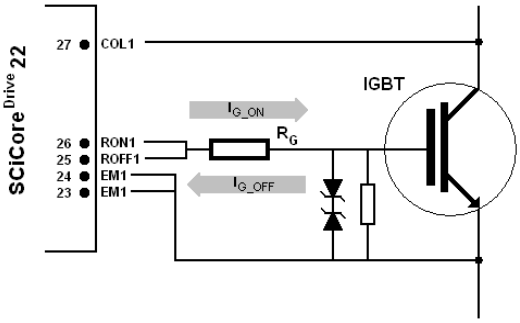


figure 9

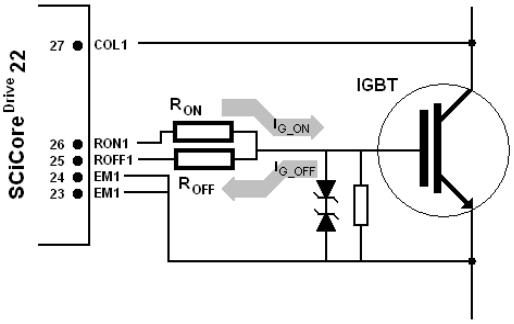


figure 10

The output stage of **SCiCoreDrive22** has two outputs for easy asymmetrical gate control. This allows to split the gate resistor into two resistors R_{ON} and R_{OFF} for turn-on and turn-off, respectively (see figure 10). This way, the most inevitable cross current from V_{G+} to V_{G-}, (I_{G_OFF}) generated in the internal BJTs of the driver (see figure 5) during turn-off can be limited. The main advantage, however, is that this solution offers the possibility of separate optimization of turn-on and turn-off with regard to turn-on overcurrent, turn-off overvoltage spikes and short-circuit behavior.

Using two different resistors for turn-on and turn-off also permits to distribute the power losses in the gate resistor.

The formulas given below are an approximation of power dissipated by the gate resistors:

$$P_{RG\_ON} \approx R_{GON} \cdot I_{G\_ONpeak} \sqrt{\frac{t_{ON} f_{SW}}{3}} \qquad P_{RG\_OFF} \approx R_{GOFF} \cdot I_{G\_OFFpeak} \sqrt{\frac{t_{OFF} f_{SW}}{3}}$$

DRIVING 2 IGBTS

More typical applications of power electronics use topologies where 2 IGBTs are forming a half bridge configuration. **SCiCoreDrive22** was designed for this purpose (drive the both IGBT in the half bridge) it is also useful to drive 2 IGBTs in any other configuration. **SCiCoreDrive22** is a dual driver that offers 2 different modes of operation: the direct mode (DM) or the Half Bridge Mode (HBM). The architecture of the power stack (IGBTs topology) will define which is the most recommended operation mode. MODE input define the operation mode of the **SCiCoreDrive22**.

DIRECT MODE

In this mode operation, **SCiCoreDrive22** works as two independent single IGBT drivers. Each channel is «blind» respect the other one. Any configuration of the power IGBTs is permitted with this mode, we can drive 2 IGBT in any position on a power stack, even we can drive the 2 IGBT (top and bottom) from a half bridge architecture, but user must be careful because the signal applied to IN_x inputs, will be transmitted to the gate of the IGBT_x without suffering timing changes (except the delay introduced by the own driver of course). Overlays of the signals IN1 & IN2 in a half bridge architecture will produce a catastrophic short-circuit in the power stack. Control system is the responsible of guarantee the correct compatibility of the signals and introduce the dead times if if required. See figure 9

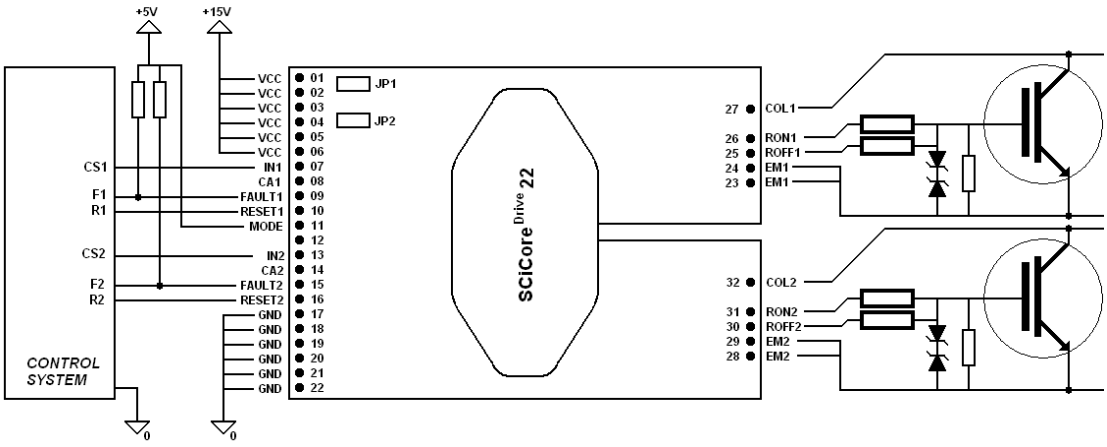


figure 11: *recommended direct mode application.*

HALF BRIDGE MODE

When we want to drive the 2 IGBT forming a half bridge, the half bridge operation mode is recommended. See figure 10. In this mode the if both signals, IN1 and IN2, are high at the same time, the intern dead time generator of the driver resolves this conflictual situation by separating the signals in time and generating automatically a dead time. This way we can assure that the signals at the output of the driver don't provoke that both IGBTs are ON at the same time. See the chronogram of the figure 11

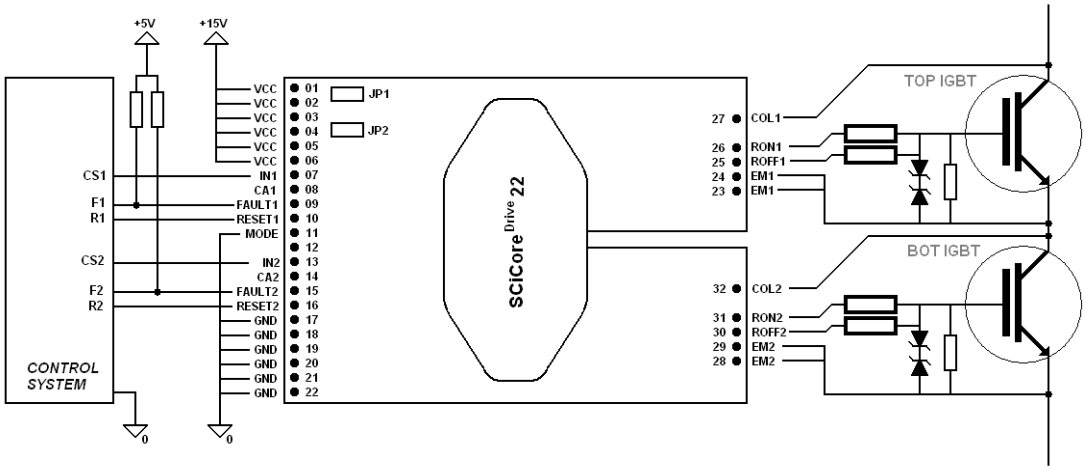


figure 12: *recommended half bridge mode application.*

The dead time between outputs of the driver is the maximum between the dead time generated by control system and the dead time generated by the driver. The minimum dead time generated by **SCiCoreDrive22** in the half bridge mode is 600 ns, if shorter dead time is required, then the direct mode must be used.

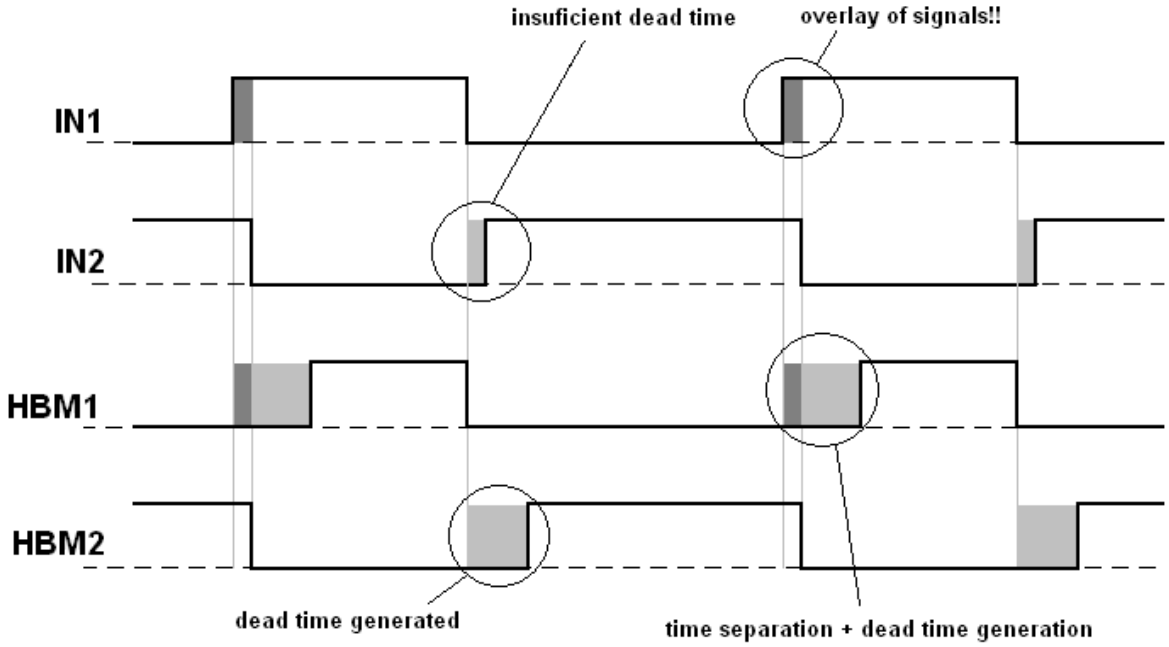


figure 13: *half bridge mode overlay signals example.*

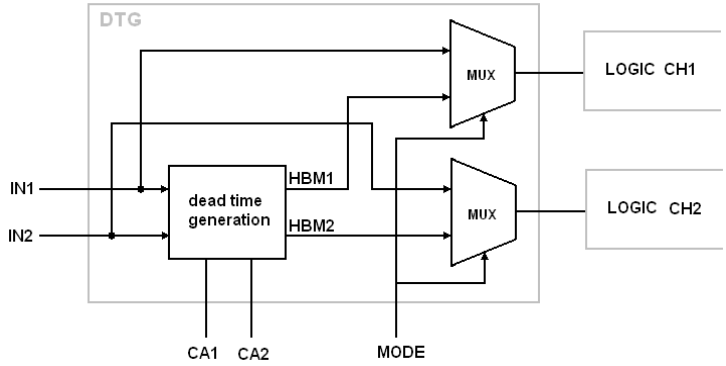


figure 14: *DTG block diagram.*

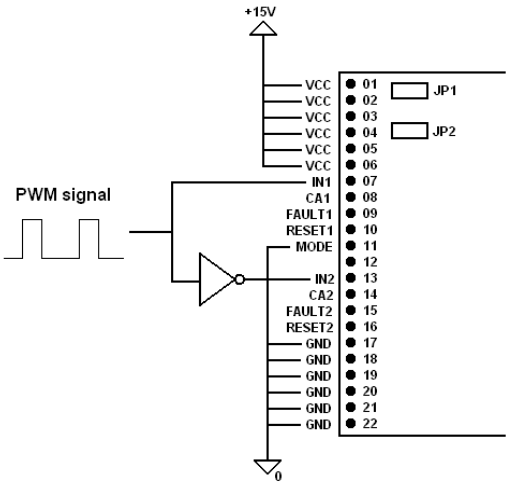


figure15: *Possible configuration with single PWM signal (HBM).*

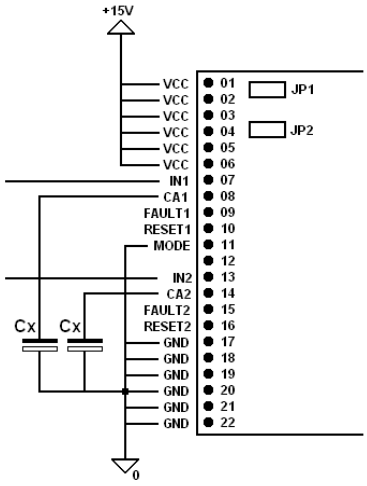


figure 16: *External capacitor connection in HBM.*

USING EXTERNAL CAPACITORS FOR INCREASE THE GENERATED DEAD TIME

The dead time generated by SCi can be increased by connecting capacitors to the pins CA1 & CA2. See figure 16. Both external capacitors connected must be of the same value, otherwise the generated dead time between channels will be unbalanced. See figure 17 for obtaining the relation between the value of the capacitors Cx and the dead time generated.

External capacitor	Dead time generated
NO EXT. CAPACITOR	600 ns
47 pF	840 ns
100 pF	1100 ns
150 pF	1350 ns
220 pF	1700 ns
330 pF	2200 ns
470 pF	2900 ns
680 pF	4000 ns
820 pF	4600 ns
1000 pF	5500 ns

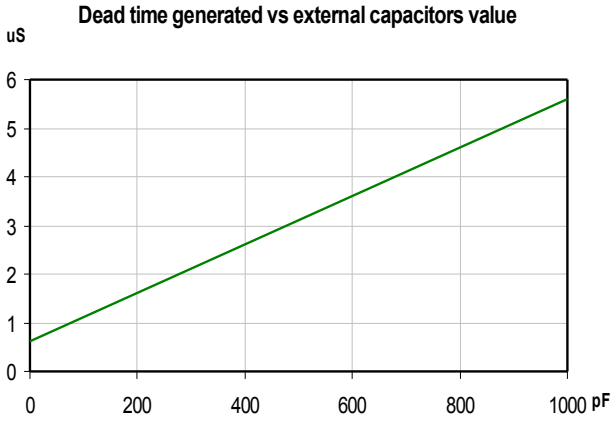


figure 17: *Dead time vs. ext. capacitor chart.*

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Tentative information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.
Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.
Advance Information: The product design is complete and final characterization for volume production is well in hand.
No Annotation: The product parameters are fixed and the product is available to datasheet specification.

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